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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte WALTER CLARK MILLIKEN, CRAIG PARTRIDGE,
and ALDEN W. JACKSON

Appeal 2008-1780
Application 09/938,921
Technology Center 2400

Decided: November 13, 2008

Before JOSEPH L. DIXON, ST. JOHN COURTENAY III, and
STEPHEN C. SIU, *Administrative Patent Judges*.

SIU, *Administrative Patent Judge*.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134(a) from the Examiner's rejection of claims 1-18 and 19-21. We have jurisdiction under 35 U.S.C. § 6(b). We affirm in part.

THE INVENTION

The disclosed invention relates generally to processing data via a central processing unit containing an embedded ternary content addressable memory device (Spec. 2).

Independent claim 1 is illustrative:

> 1. In a network device, a central processing unit (CPU) comprising:
>
> an arithmetic logic unit; and
>
> a ternary content addressable memory operatively coupled to the arithmetic logic unit within the CPU and configured to perform one or more matching operations.

THE REFERENCES

The Examiner relies upon the following references as evidence in support of the obviousness rejection:

Curtis	US 6,000,016	Dec 7, 1999
Zuraski	US 6,560,740 B1	May 6, 2003 (filed Aug. 3, 1999)
Nataraj	US 6,757,779 B1	Jun. 29, 2004 (filed Oct. 31, 2001)

THE REJECTIONS

1. Claim 21 stands rejected under 35 U.S.C. § 101 as being directed to non-statutory subject matter.
2. Claims 1-6, 8-15, and 20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Curtis and Nataraj.

3. Claims 7, 16, 18, and 19 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Curtis, Nataraj, and Zuraski.
4. Claim 21 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Zuraski and Nataraj.

PRINCIPLES OF LAW

35 U.S.C. § 103

> Section 103 forbids issuance of a patent when "the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains."

KSR Int'l Co. v. Teleflex Inc., 127 S. Ct. 1727, 1734 (2007).

"What matters is the objective reach of the claim. If the claim extends to what is obvious, it is invalid under *§ 103*." *Id.* at 1742. To be nonobvious, an improvement must be "more than the predictable use of prior art elements according to their established functions." *Id.* at 1740. Appellants have the burden on appeal to the Board to demonstrate error in the Examiner's position. *See In re Kahn*, 441 F.3d 977, 985-86 (Fed. Cir. 2006) ("On appeal to the Board, an applicant can overcome a rejection [under § 103] by showing insufficient evidence of *prima facie* obviousness or by rebutting the *prima facie* case with evidence of secondary indicia of nonobviousness.") (quoting *In re Rouffet*, 149 F.3d 1350, 1355 (Fed. Cir.

1998)). Therefore, we look to Appellants' Brief to show error in the proffered prima facie case.

FINDINGS OF FACT

The following Findings of Facts (FF) are shown by a preponderance of the evidence.

1. Curtis discloses a "bypass network **110** [that] includes a content addressable memory array (CAM) **128**" (col. 4, ll. 31-32).
2. Nataraj discloses "a ternary CAM array that stores policy statements" (col. 7, l. 46) and "is capable of locally masking each entry . . . [such that] [e]ach policy field that corresponds to a match clause . . . will be unmasked" (col. 7, l. 67 – col. 8, l. 2).
3. Zuraski discloses "a content addressable memory (CAM) 82 of repair logic unit 70" (col. 9, ll. 51-52) that "produces an asserted HIT signal" (col. 9, ll. 57-58).

ANALYSIS

35 U.S.C. § 101

We consider the Examiner's rejection of independent claim 21 as being directed to non-statutory subject matter.

The Examiner finds that "claim 21 falls under the category of a 'machine'" (Ans. 20) but nevertheless "is directed to non-statutory subject matter because it appears to <u>have no substantial practical application</u>" (*id.*). "[W]hen an abstract concept has no claimed practical application, it is not

patentable." *In re Comiskey*, 499 F.3d 1365, 1376 (Fed. Cir. 2007). However, because claim 21 "falls under the category of a 'machine'" as the Examiner finds, and is therefore not directed to "an abstract concept," we disagree with the Examiner's conclusion that claim 21 is directed to non-statutory subject matter.

Accordingly, we conclude that Appellants have met their burden of showing that the Examiner erred in rejecting claim 21 under 35 U.S.C. § 101.

35 U.S.C. § 103

Claims 1-15 and 20

We consider the Examiner's rejection of claims 1-6, 8-15, and 20 as being unpatentable over Curtis and Nataraj and of claim 7 as being unpatentable over Curtis, Nataraj, and Zuraski.

Claim 1 recites a central processing unit (CPU) comprising a ternary content addressable memory and claim 20 recites a "means for processing the packet using a ternary content addressable memory resident within a central processing unit." Appellants assert that "Curtis et al. and Nataraj et al. do not disclose or suggest means for processing the packet using a ternary content addressable memory resident within a central processing unit of the network device" (App. Br. 19).

Although the Examiner finds that Nataraj discloses that a "*policy statement table 404 is stored in a ternary CAM array*" (Ans. 28) and "*performing classifying and filtering policy statements using the ternary*

CAM 404" (id.), the Examiner does not demonstrate that Nataraj or Curtis also discloses a ternary CAM "resident within a central processing unit" or a CPU comprising a ternary CAM as recited in claim 1 or claim 20. Nor has the Examiner demonstrated that Zuraski cures the deficits of Nataraj and Curtis.

Accordingly, we conclude that Appellants have met their burden of showing that the Examiner erred in rejecting claims 1 and 20, and of claims 2-15, which depend therefrom, under 35 U.S.C. § 103.

Claims 16, 18, and 19

We consider the Examiner's rejection of claims 16, 18, and 19 as being unpatentable over Curtis, Nataraj, and Zuraski. Since Appellants' arguments have treated these claims as a single group which stand or fall together, we select dependent claim 16 as the representative claim for this group. *See* 37 C.F.R. § 41.37(c)(1)(vii).

Appellants assert that the cited references do not disclose claim 16 which ". . . specifically recites processing a packet using a ternary content addressable memory resident within an arithmetic logic unit of a network device" (App. Br. 24) because "Zuraski, Jr. et al. does not disclose . . . an arithmetic logic unit or a ternary content addressable memory" (App. Br. 24).

Nataraj discloses that a "policy statement table **404** is stored in a ternary CAM array" (col. 7, ll. 45-46). Because Nataraj discloses a ternary

content addressable memory (ternary CAM), we do not find Appellants' assertion that Zuraski does not disclose a ternary content addressable memory, even if true, to be persuasive. One cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. *In re Merck & Co., Inc.*, 800 F.2d 1091 (Fed. Cir. 1986); *In re Keller*, 642 F.2d 413 (CCPA 1981).

Appellants also argue that although Zuraski "depicts a repair logic unit 70" (App. Br. 22), "Zuraski, Jr. et al. does not disclose or suggest that repair logic unit 70 is an arithmetic logic unit" (App. Br. 24).

While the Specification describes examples of potential arithmetic logic units, the Specification nevertheless fails to provide an explicit definition. Using a broad but reasonable construction with the plain and ordinary meaning of the term, we find that an arithmetic logic unit includes any component of a computer system that carries out arithmetic and/or logic operations on computer instructions. Zuraski discloses that the "[r]epair logic unit 70 selects between the first and second DO signals to produce the DATA OUT signal" (col. 9, ll. 64-66). Because the repair logic unit of Zuraski processes data (i.e., first and second DO signals) and generates output (i.e., DATA OUT signal), we find that the repair logic unit of Zuraski performs arithmetic and/or logic operations. As such, we find that the repair logic unit of Zuraski encompasses an arithmetic logic unit. Although Appellants argue the Zuraski does not state the term "arithmetic logic unit," Appellants have failed to provide convincing arguments to demonstrate any

specific differences between the arithmetic logic unit of claim 16 and the repair logic unit of Zuraski.

Appellants further argue that "the Examiner's purported motivation to combine the cited references is merely conclusory and based on impermissible hindsight" (App. Br. 25).

Curtis discloses a computer system including content addressable memory (CAM) arrays that determine "a match between one of the source addresses and one of the destination addresses" (col. 2, ll. 41-42). Nataraj discloses a ternary CAM array that contains policy field where "[e]ach policy field that corresponds to a match clause . . . will be unmasked" (col. 8, ll. 1-2). Zuraski discloses a CAM device such that "[w]hen the address signals match the contents of a memory location within CAM 82, CAM 82 produces an asserted HIT signal" (col. 9, ll. 56-57). Thus, each of Curtis, Nataraj, and Zuraski discloses the known elements of a CAM or ternary CAM device that receives data, processes data, and detects a match. We agree with the Examiner that it would have been obvious to one of ordinary skill in the art to combine the known elements of Curtis (i.e., system containing a CAM array that determines matches between data), Nataraj (i.e., system containing a ternary CAM that unmasks a match clause), and Zuraski (i.e., a CAM that determines matches between data and generates an output signal) to achieve an expected and predictable result of a system containing a CAM or ternary CAM that detects matches between data. Appellant fails to demonstrate that the combination of these known elements

of Curtis, Nataraj, and Zuraski would have yielded anything more than what one of ordinary skill in the art would have expected from such a combination. "[W]hen a patent 'simply arranges old elements with each performing the same function it had been known to perform' and yields no more than one would expect from such an arrangement, the combination is obvious." *KSR* at 1740 (citing *Sakraida v. AG Pro, Inc.*, 425 U.S. 273, 282 (1976))

For at least the aforementioned reasons, we conclude that Appellants have not sustained the requisite burden on appeal in providing arguments or evidence persuasive of error in the Examiner's rejection of representative claim 16, or claims 18 and 19, which fall therewith, as being unpatentable over Curtis, Nataraj, and Zuraski.

Claim 21

We consider the Examiner's rejection of claim 21 as being unpatentable over Zuraski and Nataraj.

Appellants assert that "Zuraski, Jr. et al. and Nataraj et al. do not disclose or suggest an arithmetic logic unit" because "Zuraski, Jr. et al. does not disclose or suggest that BIST logic unit 20 is an arithmetic logic unit" (App. Br. 26).

In the absence of a specific definition of the term "arithmetic logic unit" in the Specification, we construe the term broadly but reasonably as described above. Zuraski discloses that the BIST logic unit contains a

"[d]ata generator **64** [that] produces data signals . . . and provides the data signals to embedded memory unit **16** . . . (and) data comparator **66**" (col. 8, ll. 52-56). We find that Zuraski's BIST logic unit 20 encompasses an arithmetic logic unit because both the BIST logic unit 20 and the arithmetic logic unit carry out arithmetic and/or logic operations on computer instructions.

Appellants also argue that "the Examiner's purported motivation to combine the cited references is merely conclusory and based on impermissible hindsight" (App. Br. 28). We disagree with Appellants' contention for reasons set forth above.

For at least the aforementioned reasons, we conclude that Appellants have not sustained the requisite burden on appeal in providing arguments or evidence persuasive of error in the Examiner's rejection of claim 21 as being unpatentable over Zuraski and Nataraj.

CONCLUSION OF LAW

Based on the analysis above, we conclude that Appellants have shown Examiner error in rejecting claim 21 under 35 U.S.C. § 101 as being directed to non-statutory subject matter and in rejecting claims 1-15 and 20 under 35 U.S.C. § 103(a) for obviousness.

However, we conclude that Appellants have not shown the Examiner erred in rejecting claims 16, 18, 19, and 21 under 35 U.S.C. § 103(a) for obviousness.

DECISION

We reverse the Examiner's decisions rejecting claim 21 under 35 U.S.C. § 101 and claims 1-15 and 20 under 35 U.S.C. § 103(a).

We affirm the Examiner's decision rejecting claims 16, 18, 19, and 21 under 35 U.S.C. § 103(a) for obviousness.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED-IN-PART

rwk

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